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IN THE CLAIMS:

Please add claims 46-56 and amend the remaining claims as follows:

Claims 1-21 (Cancelled).

22. (Currently Amended) A method of determining whether an adjacent aggressor net ~~may switch~~ switches during a victim window of a victim net in a static timing analysis of an integrated circuit design, said method comprising:

a) checking for overlap between said victim window and a switching window of said aggressor net;

b) translating said victim net to a context of each input window of said aggressor net, if said checking step identified an overlap;

c) repeating said checking for each said input window and translated victim window; and

~~d) determining that said aggressor net may switch during said victim window only if said checking step found an overlap and at least one of said repeating steps determined that said input could switch during said translated victim window~~

if said checking step identifies an overlap:

determining an initial set of aggressor sub-windows; and

merging said aggressor sub-windows of said initial set into a final set of aggressor sub-windows.

wherein said repeating process checks for overlap between said translated victim window and each of said final set of aggressor sub-windows.

23. (Currently Amended) The method of claim 22, wherein said repeating step is repeated only for a limited number of levels of sub-windows.

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24. (Canceled).

25. (Currently Amended) The method of claim 22 24, wherein said repeating process checks for overlap between each said aggressor sub-window and a related translated victim window.

26. (Currently Amended) ~~The method in claim 22, further comprising,~~ A method of determining whether an adjacent aggressor net switches during a victim window of a victim net in a static timing analysis of an integrated circuit design, said method comprising:

a) checking for overlap between said victim window and a switching window of said aggressor net;

b) translating said victim net to a context of each input window of said aggressor net, if said checking step identified an overlap;

c) repeating said checking for each said input window and translated victim window; and

d) determining that said aggressor net can switch during said victim window only if said

a) checking step found an overlap and at least one of said repeating steps determined that said input window could switch during said translated victim window and;

if said checking step identified an overlap:

determining an initial set of aggressor sub-windows; and

merging said aggressor sub-windows of said initial set into a final set of aggressor sub-windows,

wherein said repeating process checks for overlap between said translated victim window and each of said final set of aggressor sub-windows.

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27. (Original) The method in claim 22, wherein said method is performed in a direction in which signals travel through said integrated circuit.

28. (Original) The method in claim 22, wherein said method is performed in a direction opposite that in which signals travel through said integrated circuit.

Claims 29-45 (Cancelled).

46. (New) The method of claim 26, wherein said repeating step is repeated only for a limited number of levels of sub-windows.

48. (New) The method of claim 26, wherein said repeating process checks for overlap between each said aggressor sub-window and a related translated victim window.

49. (New) The method in claim 26, wherein said method is performed in a direction in which signals travel through said integrated circuit.

50. (New) The method in claim 26, wherein said method is performed in a direction opposite that in which signals travel through said integrated circuit.

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51. (New) A method of determining whether an adjacent aggressor net switches during a victim window of a victim net in a static timing analysis of an integrated circuit design, said method comprising:

checking for overlap between said victim window and a switching window of said aggressor net; and, if said overlap is identified:

determining an initial set of aggressor sub-windows;

merging said aggressor sub-windows of said initial set into a final set of aggressor sub-windows; and

checking for overlap between said victim window and each item in said final set of aggressor sub-windows.

52. (New) The method of claim 51, wherein each said switching window of said aggressor net comprises at least one aggressor sub-window.

53. (New) The method of claim 52, wherein said repeating step is repeated only for a limited number of levels of sub-windows.

54. (New) The method of claim 52, wherein said repeating process checks for overlap between each said aggressor sub-window and a related victim window.

55. (New) The method in claim 51, wherein said method is performed in a direction in which signals travel through said integrated circuit.

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56. (New) The method in claim 51, wherein said method is performed in a direction opposite that in which signals travel through said integrated circuit.